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UNITED STATES LETTERS PATENT APPLICATION

FOR

**A THERMAL CONDUCTING TRENCH IN A SEMICONDUCTOR
STRUCTURE AND METHOD FOR FORMING THE SAME**

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**A THERMAL CONDUCTING TRENCH IN A SEMICONDUCTOR
STRUCTURE AND METHOD FOR FORMING THE SAME**

RELATED APPLICATION

[0001] The application is a continuation application of co-pending U.S. Patent Application, Serial No. 09/791,054, filed February 21, 2001, by applicants, Chunlin Liang and Brian S. Doyle, entitled "A Thermal Conducting Trench in a Semiconductor Structure and Method for Forming the Same;" which is a divisional application of co-pending U.S. Patent Application, Serial No. 08/829,860, filed on March 31, 1997, by applicants, Chunlin Liang and Brian S. Doyle, entitled "A Thermal Conducting Trench in a Semiconductor Structure and Method for Forming the Same."

BACKGROUND

Field

[0002] The invention relates generally to the field of semiconductor devices and, more particularly, to dissipating heat generated by the operation of such devices.

Description of Related Art

[0003] One goal of complementary metal oxide semiconductors (CMOS) in very large scale integration (VLSI) and ultra large scale integration (ULSI) is to increase chip density and operation speed. However, with increased chip density and operation speed, CMOS power consumption is also increased dramatically. It is expected that the power consumption of a high performance microprocessor will increase from several watts currently to approximately several hundred watts in the near future. The heat generated from this power consumption will raise chip temperature dramatically and degrade circuit performance and reliability. Therefore, reducing chip operation temperature is of great importance for current as well as future VLSI and ULSI technology.

[0004] To date, reduction of chip temperature is accomplished in two ways: 1) Lowering the power consumption, and 2) improving heat dissipation to the ambient environment. The first method is the preferred approach. A

lowering of the power consumption is usually accomplished by scaling down the power supply voltage. The power consumption of integrated circuit chips has decreased from 5.0 volts several years ago to today's approximately 1.5 volts. However, lowering of the power supply voltage may impact negatively on the performance of the device. Because of the non-scalability of the built-in voltage of a silicon junction, there is little room for further reduction of the power supply voltage below 1.0 volts if traditional technology is used. Thus, for high performance VLSI and ULSI circuits, further lowering of the power supply voltage may not be the most effective approach.

[0005] As indicated previously, the second approach to the reduction of chip temperature is through improved heat dissipation to the ambient environment. The heat dissipates mainly through the silicon substrate into a metal heat sink inside the package and through a metal interconnect system. This approach typically employs a heat sink/ground plan in physical contact with the silicon substrate. Some modern technologies, however, have eliminated the heat sink/ground plan in physical contact with the silicon substrate. One example is flip-chip technology wherein the chip is inverted so that the interconnect system lies on the underside of the chip rather than on the exposed top surface. These technologies encapsulate the silicon chip inside a package with epoxy material thus eliminating the contact between the silicon substrate and a heat sink. Instead, the metal interconnect system becomes the dominant heat dissipation path.

[0006] Heat dissipation through the interconnect system may be improved by increasing the total physical contact area to a heat source. A large effective physical contact area will reduce the thermal resistivity proportionally. In a typical chip design, the primary effective thermal contact to the transistor is provided by the diffusion or source/drain contact. The total source and drain physical contact area is, however, limited to a small percentage of the total chip size because other structures, such as an active channel, isolation, metal interconnect, and separation space, consume a much larger area of a given chip. Thus, the current design of the thermal contact area to the transistor (i.e., the area available to effectively dissipate heat

generated by the transistor) is insufficient to dissipate the heat generated by the power consumption anticipated for future CMOS technology.

SUMMARY

[0007] A method of forming a trench filled with a thermally conducting material in a semiconductor substrate is disclosed. In one embodiment, the method includes filling a portion of the trench with a thermally conducting material and patterning a contact to the thermally conducting material. A semiconductor device is also disclosed. In one embodiment, the semiconductor device has a trench defining a cell region, wherein a portion of the trench includes a thermally conducting material, and a contact to the thermally conducting material. A semiconductor device and a method of forming a semiconductor device with an interlayer dielectric that is a thermally conducting material is further disclosed.

[0008] Additional features and benefits of the invention will become apparent from the detailed description, figures, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **Figure 1** is a schematic diagram of a portion of a semiconductor substrate showing a masking layer overlying the substrate and a trench formed in the substrate for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0010] **Figure 2** is a schematic diagram of a portion of an integrated circuit structure showing a dielectric material passivating the sidewalls of the trench and overlying the masking layer for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0011] **Figure 3** is a schematic diagram of a portion of an integrated circuit structure showing a thermally conducting material overlying the passivating dielectric layer and filled in the trench for an embodiment of an

integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0012] **Figure 4** is a schematic diagram of a portion of an integrated circuit structure showing the thermally conducting material filled in the trench and removed from the surface of the substrate by using the masking layer as an etch stop for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0013] **Figure 5** is a schematic diagram of a portion of an integrated circuit structure showing the masking layer removed for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0014] **Figure 6** is a schematic diagram of a portion of an integrated circuit structure showing a transistor structure formed adjacent to the trench and conductive interconnections to the transistor and the trench for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0015] **Figure 7** is a schematic view of a portion of an integrated circuit structure showing six transistor devices and thermally conducting dielectric material filled trench/trench isolation for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0016] **Figure 8** is a schematic view of a portion of an integrated circuit structure showing power (e.g., V_{CC} and V_{SS}) bus metal lines also used as the thermal connection to the thermally conducting material in the trench for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0017] **Figure 9** is a schematic view of a portion of an integrated circuit structure showing the regular electrical metal interconnections used as thermal connections to the thermally conducting material in the trench for an embodiment of an integrated circuit structure having a trench filled with a thermally conducting material in the semiconductor substrate in accordance with the invention.

[0018] **Figure 10** is a schematic view of a portion of an integrated circuit structure showing dielectric sidewall spacers formed between opposing metal interconnect lines for an embodiment of the invention of an integrated circuit structure having an interlayer thermally conducting dielectric material in accordance with the invention.

[0019] **Figure 11** is a schematic view of a portion of an integrated circuit structure showing a layer of thermally conducting dielectric material deposited over a first level metal interconnect system for an embodiment of the invention of an integrated circuit structure having an interlayer thermally conducting dielectric material in accordance with the invention.

[0020] **Figure 12** is a schematic view of a portion of an integrated circuit structure showing a planarized thermally conducting dielectric material between opposing metal interconnect lines for an embodiment of the invention of an integrated circuit structure having an interlayer thermally conducting dielectric material in accordance with the invention.

[0021] **Figure 13** is a schematic view of a portion of an integrated circuit structure showing an interlayer dielectric deposited over the structure to passivate the metal line and the thermally conducting dielectric material for an embodiment of the invention of an integrated circuit structure having an interlayer thermally conducting dielectric material in accordance with the invention.

[0022] **Figure 14** is a schematic view of a portion of an integrated circuit structure showing an embodiment of the invention with a transistor device adjacent to a trench filled with thermally conducting dielectric material in accordance with the invention.

[0023] **Figure 15** is a schematic view of a portion of an integrated circuit structure showing an embodiment of the invention wherein thermally conducting dielectric material overlies the structure and metal contacts are established to the diffusion regions in accordance with the invention.

[0024] **Figure 16** is a schematic view of a portion of an integrated circuit structure showing an embodiment of the invention wherein the interlayer dielectric layer is replaced with thermally conducting dielectric material in accordance with the invention.

DETAILED DESCRIPTION

[0025] Embodiments in accordance with the present invention include a semiconductor device and a method for forming a semiconductor device having a trench with a portion of the trench filled with a thermally conducting material defining a cell or active region. Embodiments in accordance with the invention also include a semiconductor device and a method for forming a semiconductor device having a trench with a portion of the trench filled with a thermally conducting material defining a cell or active region and a contact to the thermally conducting material. Embodiments in accordance with the invention further include a semiconductor device and a method for forming a semiconductor device with an interlayer dielectric that is a thermally conducting material. Embodiments of the device and process for making the device allow for improved heat dissipation across a chip.

[0026] In one embodiment, a thermal conducting trench filled with a thermally conducting material is embedded in the chip active layer very close to the heating source, e.g., the transistor. The thermally conducting trench may be constructed throughout the isolation region and may provide sufficient extra thermal contact area in addition to those contributed from electrical source/drain contacts, so that sufficient heat may be dissipated without adding extra space. Therefore, the thermal conducting channel filled in the active layer provides additional thermal contact area and significantly relieves the thermal heating problem with little penalty on chip size or process complexity. In another embodiment, thermally conducting material is used as a replacement for part or all of the interlayer dielectric to improve the heat dissipation in higher level structures.

[0027] In the following description, numerous specific details are set forth such as specific materials, thicknesses, processing steps, process parameters, etc., in order to provide a thorough understanding of the invention. One skilled in the art will understand that these specific details need not be employed to practice the invention.

[0028] **Figures 1-6** illustrate schematically an embodiment of a method of forming a semiconductor structure in accordance with the invention. **Figure 1** illustrates the formation of trenches 150 in silicon substrate 100. The trenches filled with a thermally conducting material are formed using conventional trench isolation techniques. In this trench isolation process, a masking layer 110, such as for example, a silicon nitride (Si_xN_y) masking layer 110, is deposited over silicon substrate 100 to protect substrate 100 from a subsequent etchant and to define a trench or trench pattern. Next, the structure is exposed to a suitable etchant to form trench 150 in the silicon substrate. The etching of trench 150 may be carried out by a chlorine etch chemistry, such as for example, BCl_3/Cl_2 , $\text{H}_2/\text{Cl}_2/\text{SiCl}_4$, and $\text{CHCl}_3/\text{O}_2/\text{N}_2$, or other suitable etch chemistry as known in the art.

[0029] Trench 150 may be used to define an active region, for example isolating n^+ and p^+ regions in CMOS circuits. The trench depth may vary, but typically is approximately uniform across the semiconductor substrate 100 and determined by the particular requirements of the structure. In CMOS technology, such trenches 150 typically range from a depth of $0.4\ \mu\text{m}$ to greater than $3\ \mu\text{m}$.

[0030] Next, as shown in **Figure 2**, a dielectric interface layer 120 is formed over the masking layer 110 and adjacent to the sidewalls and base of the trench 150. Interface layer 120 may be deposited by conventional techniques, e.g., chemical vapor deposition of dielectric material, or may be grown, e.g., thermal SiO_2 . Interface layer 120 seals off the exposed silicon in the trench and passivates the trench. Interface layer 120 serves as an interface between silicon substrate 100 and the thermally conducting material that will ultimately be filled in the trench. Interface layer 120 serves to prevent any trench leakage between devices isolated by the trench 150.

[0031] In some embodiments, interface layer 120 thickness may be limited. The thicker interface layer 120, the higher the thermal resistivity between silicon substrate 100 and material in the trench 150. The thermal resistivity of trench 150 is increased by a thicker interface layer 120, because the heat that is given off by an adjacent device, for example, is impeded from

traveling to the thermally conducting material by interface layer 120. An interface layer 120 of SiO_2 , for example, of 300 Å or less may be appropriate to impart the desirable properties of an interface and suitable thermal resistivity. It is to be appreciated, however, that various dielectric materials of various thicknesses may be used as an interface layer 120. Further, if channel leakage is not a concern, the interface layer 120 may be eliminated.

[0032] After interface layer 120 is formed in trench 150, **Figure 3** illustrated a thermal conducting layer 130 deposited over the substrate and into trench 150. The layer 130 should also be electrically insulating. Thermally conductive material is material that transfers heat from one point to another. In this context, a thermally conductive material is a material that transfers or conducts heat and may be distinguished, for example, by those materials that primarily insulate, like conventional semiconductor dielectrics such as SiO_2 or Si_xN_y . High thermal conductivity is a thermal conductivity greater than 0.2 W/cmK. Of course, the invention is not limited to utilizing materials that have high thermal conductivity. Thermally conductive materials suitable for use in the invention include, but are not limited to, AlN, BN, SiC, polysilicon, and chemical vapor deposited (CVD) diamond. Table I compares the thermal conductivities of ordinary dielectrics of SiO_2 and Si_xN_y with these thermally conducting materials and copper metal.

Table I. Thermal Conductivity (W/cm K):

SiO_2	Si_3N_4	SiC	Poly Si	AlN	BN	Diamond	Cu
0.014	0.185	0.38	1.412	1.8-3.2	3.5-4.5	12-23	2.0-5.0

[0033] As shown in **Figure 4**, a chemical-mechanical polishing step, suitable for thermally conducting material 130, is next used to polish away thermally conducting material 130 from the substrate surface leaving thermally conducting material 130 only in trench region 150. The chemical mechanical polish is accomplished using the dielectric layer (e.g., Si_xN_y) 110 as an etch stop. In other words, both thermally conducting material 130 and interface layer 120 are removed from the upper surface of the substrate 100 but remain in trench 150. Though the removal of thermally conducting material 130 from

the surface of the substrate is described herein as a chemical-mechanical polishing step, it is to be appreciated that excess thermally conducting material 130 may be removed by way of other techniques, such as for example, conventional etching techniques.

[0034] Next, as shown in **Figure 5**, the dielectric/etch stop layer 110 is removed from the substrate surface using standard dry etching techniques. For example, a Si_xN_y etch stop layer is removed using, for example, a CHF_3/O_2 etch chemistry. The same etch stop layer may alternatively be removed by wet etching, such as for example, by hot phosphoric acid.

[0035] With the thermally conducting trench formed, conventional fabrication processes may be used to formulate the integrated circuit structures on the substrate. A schematic side view of a portion of an integrated circuit structure is shown in **Figure 6**. In **Figure 6**, a transistor is formed in the cell or active region defined by trench 150 of substrate 100. The transistor consists of a gate 140 that is, for example, doped polysilicon, overlying a gate oxide 170 and adjacent to n^+ or p^+ diffusion regions 160 in substrate 100 that is of the opposite dopant of diffusion regions 160. Adjacent gate 140 are sidewall dielectric spacers 180. Sidewall spacers 180 may comprise virtually any dielectric, including a single oxide or silicon nitride (Si_xN_y) or several layers formed by various methods. For example, one or more layers of oxide may be deposited by plasma-enhanced chemical vapor deposition ("PECVD"), thermal CVD, atmospheric pressure CVD, and subatmospheric pressure CVD. An interlayer dielectric (ILD) material 195 is deposited and contact holes are formed to permit discrete metal contacts diffusion regions 160 and trenches 150. Finally, **Figure 6** shows contact 196 to gate 140 and interlayer dielectric 195 and 200, respectively, isolating the electrical/thermal interconnect systems.

[0036] As noted above, a metal interconnect 190, that is, for example, aluminum, is deposited to the diffusion regions 160 to form an electrical interconnection between the diffusion regions of the transistor and the integrated circuit. A similar conductive interconnection is patterned to the thermally conducting material 130 in trench 150. In one embodiment, interconnect 190 is patterned to diffusion region 160 and thermally conducting

material 130. In other words, electrical interconnect system 190 may be used as a thermal interconnect system for heat transfer purposes as well as electrical interconnect purposes. The thermally conducting material 130 in this embodiment should be electrically insulating to prevent shorting problems. It should, however, be appreciated, that the thermal interconnect system and the electrical interconnect system need not be the same. Instead, separate or discrete interconnect systems may be established for electrical and thermal purposes. Further, in an embodiment utilizing thermal conducting material 130 having thermal conductivities greater than 1.8 W/cmK, no contact to thermally conducting material 130 is necessary.

[0037] To form interconnect system 190 that is to be used as both an electrical interconnect system and a thermal interconnect system, a masking layer is deposited over dielectric layer 195 exposing areas that will become vias or openings to thermally conducting material 130 and diffusion regions 160. Next, the via or openings to thermally conducting material 130 and diffusion regions 160 are formed by conventional etching techniques. For example, a tetraethylorthosilicate (TEOS) SiO₂ dielectric layer 195 is anisotropically etched with a CHF₃/O₂ etch chemistry to form vias or openings to thermally conducting material 130 and diffusion regions 160. Once the vias or openings are formed to thermally conducting material 130 and diffusion regions 160, the masking layer is removed and a metal, for example aluminum, is patterned concurrently to both thermally conducting material 130 and diffusion regions 160.

[0038] The introduction of a trench filled with thermally conducting material significantly improves the thermal dissipation of the chip with little, if any, negative impact on performance in process. Thus, heat generated, for example, by a transistor device may be transferred to the thermally conducting material and then transferred away from the individual device, by transfer through the thermally conductive material itself or, in the embodiment where there is a contact to the thermally conductive material, through the contact, and, optionally, through a heat sink connected to the interconnect system.

[0039] It is generally accepted, for example, that dielectric materials with high thermal conductivity, such as would be suitable for use in the invention, generally will have a high dielectric constant which will tend to increase the inter-metal capacitance and slow down a device. Because the thermally conducting material is embedded in the semiconductor substrate there is little or no negative effect on the circuit speed. Further, once the trench with the thermally conducting material is in place, the modifications to the conventional semiconductor processing steps are not significant, notably the patterning of a metal contact to the trench. However, since the electrical metal interconnect system can be used also as the thermal interconnect system as shown in **Figure 6**, the process steps of patterning the metal to the trench are not significant. Further, since the optional interface dielectric layer along the sidewalls of the trench is as thin as 300 Å or less, thermal conduction between the active transistor and the thermally conducting material 130 is achieved.

[0040] **Figure 7** is a schematic top view illustrating an embodiment of an integrated circuit structure with thermally conducting material filled trench isolation. In **Figure 7**, thermally conducting material 130 forms a filled thermal conduction network across chip 250. **Figure 7** shows six transistors 230 including a gate 140 with diffusion regions 160. Each of the six transistors 230 is isolated from one another by a trench filled with a thermally conducting material 130. Metal interconnects 190 are patterned to the diffusion regions. Electrical interconnections 190 are coupled to bus lines 210 and 220, respectively (for example, VCC and VSS bus lines). A further electrical contact 196 is patterned to gate 140 of each active transistor 230.

[0041] **Figure 8** is a schematic top view of a portion of an integrated circuit structure wherein the electrical interconnect system is also used for heat transfer purposes. In **Figure 8**, bus lines 210 and 220, respectfully, are patterned to the thermally conducting material 130. Patterning to thermally conducting material 130 is illustrated by contacts 215 on the bus lines. In this manner, the heat conducted from the transistor 230 to the thermally conducting material 130 can be dissipated through the metal interconnect system to, for example, an external heat sink (not shown). Since thermally conducting material 130 is thermal conducting and electrically insulating, the

same electrical interconnect system can be used for heat transfer purposes. The structure shown in **Figure 9** includes contacts 215 to the bus lines as well as contacts 217 to other metal interconnect of the circuit to further enhance the heat dissipation capacity of the circuit.

[0042] Compared with replacing all of the interlayer dielectric material with thermally conducting material, the approach of the previous embodiments of the invention does not raise interconnect loading capacitance significantly. Further, these embodiments do not require dedicated thermal interconnect systems or any additional chip density. These embodiments also provide more contact area between the metal interconnect and the heating source, e.g., the active transistor.

[0043] **Figures 10-14** are schematic side views of an embodiment of a process of forming further embodiments of the invention wherein thermally conducting material replaces the interlayer dielectric material of the circuit. Because the thermally conducting material will replace interlayer dielectric material, the thermally conducting material should also be electrically insulating. The following described embodiments may be used where a small increase in interconnect coupling capacitance could be tolerated. It is to be noted that the process described herein to create a structure with interlayer thermally conducting material may or may not be used in conjunction with the thermally conducting substrate trenches described above.

[0044] The introduction of thermally conducting material between interconnect lines may be incorporated into the process described above with respect to **Figures 1-6** and wherein the electrical interconnect 190 doubles as a thermal interconnect. **Figure 10** shows that, after interconnect line 190 patterning to diffusion regions 160 and thermally conducting material 130, a dielectric layer, for example, a conformal oxide, is deposited and sidewall spacers formed by a conventional anisotropic etching technique to form interface spacer portions 185 between adjacent electrical interconnect structures 190. For example, SiO₂ spacer portions 185 of between 500-1,000 Å may be formed.

[0045] **Figure 11** shows that once interface spacer portions 185 are formed, a thermally conducting material 260 is deposited over the structure in a similar manner as was done with respect to **Figure 3**, supra. Further, in the case where interlayer thermally conducting material 260 is used in connection with a substrate with thermally conducting material-filled trenches, thermally conducting material 260 can be the same as thermally conducting material 130 filled in substrate trenches.

[0046] The deposition of thermally conducting material 260 is followed by a chemical-mechanical polish process to planarize the structure and polish thermally conducting material 260 back, using metal interconnect 190 for end point detection. An etching process may also be substituted for the chemical-mechanical polish process. In this manner, as shown in **Figure 12**, thermally conducting material 260 remains in the region adjacent distinct electrical interconnect lines 190 forming a thermally conducting inter-metal trench 260 separated by dielectric sidewall spacer portions 185. A standard interlayer dielectric 270, for example a TEOS or PTEOS SiO₂, is then deposited over the structure as shown in **Figure 13**. The same or similar process as described in **Figures 10-13** may be repeated for higher level interconnects.

[0047] Where interconnect capacitance is of less concern, the interlayer dielectric may be completely replaced with thermally conducting dielectric material as shown in **Figures 14-16** wherein thermally conducting material 280 and 290 that is also electrically insulating is deposited adjacent electrical interconnect system 190. This structure may be achieved by substituting the deposition of dielectric material that would otherwise isolate the patterned metal lines with the thermally conducting dielectric material described above with reference to other embodiments of the invention. **Figure 14**, shows a schematic side view showing a transistor formed in an active region of a substrate and trenches filled with thermally conducting material 130 adjacent the transistor device and a spacer layer 180 around the gate. As shown in **Figure 15**, thermally conducting dielectric layer 290 overlies the structure and metal interconnect lines 190 are patterned to diffusion regions 160. **Figure 15** also shows interconnect lines adjacent distinct electrical interconnect lines 190 isolated from one another by sidewall spacers 185. Finally, in **Figure 16**, a layer

of thermally conducting material 280 that is also electrically insulating overlies the structure.

[0048] By introducing a trench filled with thermally conducting material, the thermal dissipation of the chip may be significantly improved with little, if any, negative impact on performance and process. By extending the use of the thermally conducting material to inter-metal space, the embodiments in accordance with the invention further improve both heat dissipation and temperature uniformity across the chip.

[0049] Due to the use of thermally conductive material in accordance with the invention, thermal equilibrium across the chip can be achieved much faster than conventional structures to provide a temperature distribution across the chip that is more uniform. This results in a more reliable electromigration of the interconnect system. The thermally conducting material utilized in accordance with the invention also helps to dissipate heat from the transistor to the surface of the structure.

[0050] In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.